

Nazmul Haque Turja

<https://nh-turja.github.io/>

Email : nh.turja@gmail.com

Mobile : +1 (575)-249-9115

Address: Folsom, CA, USA

EDUCATION

- **New Mexico State University** Las Cruces, NM
Doctor of Philosophy (PhD.) in Electrical and Computer Engineering Aug 2026 – Current
- **New Mexico State University** Las Cruces, NM
Master of Science (MSc.) in Electrical Engineering Aug 2021 – May 2023
- **Bangladesh University of Engineering and Technology (BUET)** Dhaka, Bangladesh
Bachelor of Science (BSc.) in Electrical and Electronic Engineering (EEE) Jul 2014 – Apr 2019
Major: Communication Engineering

EXPERIENCE

- **Intel Corporation** Folsom, California
GPU Logic Design Engineer Jul 2023 - Sep 2026
 - **Pre-Silicon Verification:** Conducting functional pre-silicon verification for Intel discrete, integrated, and high-performance computing (HPC) GPUs, specializing in 3D render and compute pipelines.
 - **Intel Xe-Core Management:** Owning end-to-end validation for IP features by developing test plans, creating tests, and achieving comprehensive coverage closure for next-generation ray tracing and texture sampling features, ensuring feature robustness and performance.
 - **Validation and Debugging Expertise:** Performing comprehensive validation within Intel Graphics Raytracing subsystems, leveraging UVM methodologies to deepen understanding of architectural design principles. Executing functional debugging of regression failures in simulation and emulation environments; collaborating with design and architecture teams to resolve issues effectively.
- **Department of ET and SE, New Mexico State University** Las Cruces, NM
Graduate Assistant Jan 2023 - May 2023
 - **Course Instructor:** Instructed Communication Systems I (ET 314) through theory and lab sessions, mentored students on weekly assignments and projects, and facilitated interactive discussions to enhance understanding and encourage idea exchange.
- **Intel Corporation** Folsom, California
Graduate Technical Intern May 2022 - Dec 2022
 - **Power Analysis:** Addressed critical power run issues during power flow analysis (ptpx) to develop best-in-class low-power designs for Intel Xe-Core Samplers.
 - **Regressions and Debugging:** Managed regressions for Meteor Lake (MTL) Sampler CLT's OOO feature and identified two Silicon hangs.
 - **UVM Testbench Proficiency:** Created UVM testbenches using core components and gained proficiency in *gnr*, *elab*, and *runsim* tools.
- **Department of ECE, New Mexico State University** Las Cruces, NM
Graduate Research and Teaching Assistant Aug 2021 - May 2022
 - **Basic Block Count with ML techniques:** Utilizing the nvbit supported PPT-GPU (Performance prediction toolkit for GPU), predicted the BB counts of different Polybench, Rodinia, Pannotia benchmarks, and Lulesh applications using ML techniques. (Paper Under Review)
 - **PPT-GPU:** Collaborated with **Los Alamos National Lab** for developing reuse distance and memory tracing toolkits for PPT-GPU. **GitHub:** <https://github.com/lanl/PPT>
 - **LDMS Sampler:** Associated with **Sandia National Lab** for developing Lightweight Distributed Metric System (LDMS) GPU Sampler toolkit (a modular system for HPC data collection) for IBM Power9 processor. **GitHub:** <https://github.com/ovis-hpc/ovis>
 - **Course Instructor:** Managed 50+ students on concepts of Electronics, Digital Circuit Design and VHDL and also mentored them in weekly assignments and projects with lively discussions and exchange of ideas to enhance learning.
- **Department of CSE, BRAC University** Dhaka, Bangladesh
Adjunct Faculty Feb 2021 - Sept 2021
 - **Achievement:** Conducted theory and lab classes for VLSI Design (CSE 460), and Digital Electronics and Pulse Techniques (CSE 350). These labs involve Proteus, Quartus II, Microwind and ModelSim.
 - **IoT Applications:** Involved in several applications of Internet of Things(IoT) for health-care and agriculture for the People's Republic of Bangladesh under the supervision of Dr. Farhad Hossain, Professor, department of EEE, BUET. **GitHub:** <https://github.com/nh-turja/internet-of-things>

- **Nelsite Inc. Ltd.**

Semiconductor Engineer

Fukuoka, Japan

Nov 2019 - April 2020

- **Embedded Systems:** Worked on 32 bit ARM Cortex-M4 microcontroller using keil compiler and embedded C language.
- **Semiconductor Industrial Training:** Received on-job training on basic fabrication, material characterization and the current technological trends of the semiconductor industries of Japan.

SELECTED COURSEWORK

- **Computer Engineering:** Advanced Computer Architecture, Application of Parallel Programming, ASIC Design, Hardware and Software Co-design, Compiler Transition, Computer Architecture, VLSI, Microprocessor and Interfacing, Analog and Digital Electronics.
- **Artificial Intelligence:** Application of Machine Learning, Deep Learning, Random Signal Analysis, Linear Algebra, Probability and Statistics.

PROGRAMMING SKILLS

- **Languages:** CUDA, OpenCL, Python, Embedded C/C++, VHDL, System Verilog, Golang, Lex, Yacc, LaTeX
- **Software and Tools:** Verdi, UVM, Numpy, Pandas, Tensorflow, Keras, Scikit-learn, Linux, Eagle, Proteus, Quartus II, Cadence, OpenCV

MASTER'S TECHNICAL REPORT

- **Utilizing CPI Breakdown for Bottleneck Analysis of Power9 Processor Performance:** My technical report introduces the Lightweight Distributed Metric System Sampler (LDMS-Sampler) as a comprehensive framework for CPI Breakdown analysis and pinpointing bottlenecks in IBM Power9 Processor. **Technical Report Link:** <https://tinyurl.com/cpibreakdown>

BACHELOR'S THESIS

- **A Secured Offline Online Approach for Internet of Things(IoT) Using Real-time Database:** My thesis presents several IoT applications along with a new cyber-secured MQTT based offline system that can automate various systems integrated into a single dashboard where monitoring and controlling can be simultaneously executed. **Thesis Book Link:** <https://tinyurl.com/y2n2qemu>

PROJECTS

- **Design Validation using ASMD Diagram:** Debugged and verified hardware design using Algorithmic State Machine with Data Path Diagram. **GitHub:** https://github.com/nh-turja/asmd_diagram_hw_sw_co-design_project
- **Cache Memory Simulator:** Using C++, wrote various programs for Cache Memory Simulator, which can be used for simulating different types of caches (direct mapped, set associative, etc.) **GitHub:** <https://github.com/nh-turja/cache-simulator>
- **MIPS:** Created an MIPS by using Abstract Syntax Tree (AST) for the course of Compiler Transition. **GitHub:** <https://tinyurl.com/39dyv6zv>
- **8-bit Simple As Possible(SAP) Computer:** Designed an 8-bit microcomputer with 64kBytes of main memory(RAM) support and simulated it in Proteus software. **GitHub:** <https://github.com/nh-turja/simple-as-possible-computer>
- **4-bit Shift Register:** Designed a general-purpose 4-bit shift register that is capable of left shift, right shift, and parallel loading.
- **Wearable device for Alzheimer's Patient:** Made a wearable device for Alzheimer's patients for path finding in a house. **GitHub:** <https://tinyurl.com/y4mza8h9>

PUBLICATIONS

- Nahian Ibn Hasan, Md. Tasnimul Hasan, Nazmul Haque Turja, Rishad Raiyan, Shuvagata Saha, Md Farhad Hossain. 2019. **A Cyber-Secured MQTT based Offline Automation System.** *International Conference on Wireless Communications Signal Processing and Networking (WiSPNET).*
- Shamminuj Aktar, Hamdy Abdelkhalik, Nazmul Haque Turja, Yehia Arafa, Atanu Barai, Nishant Panda, Gopinath Chennupati, Nandakishore Santhi, Stephan Eidenbenz, Abdel-Hameed Badawy. 2023. **BB-ML: Basic Block Performance Prediction using Machine Learning Techniques.**
- Nazmul Haque Turja, Hamdy Abdelkhalik, Jeanine Cook, Omar Aaziz, Abdel-Hameed Badawy. 2024. **Utilizing CPI Breakdown for Bottleneck Analysis of Power9 Processor Performance.**

AWARDS

- **Battle of Hardware (IoT):** Champion at Battle of Hardware (IoT) in "CSE Festival 2018" organized by Department of CSE, BUET.
- **CISCO Hackathon, BD:** Honorable mention at the Hackathon of the Internet of Things (IoT) organized by CISCO, Bangladesh in 2018.